ramp in compound semiconductor and wide bandgap chip production.

However, they are limited by the patterning challenges of conventional optical lithography. High-productivity e-beam litho systems that deliver next-generation resolutions, greater depth of focus (DoF) capabilities for bowed wafers with high topography, better line edge roughness (LER), and the flexibility of direct-wafer writing can meet these challenges, allowing for seamless, sustainable, rapid development and production at high volumes.

The Future is Bright for the Photomask Industry

JAN WILLIS, Co-founder, eBeam Initiative

The photomask industry is experiencing a wave of optimism as it continues to play a bigger role in supporting semiconductor scaling efforts through innovations in mask designs, materials and equipment. Combined with semiconductor growth markets of automotive, AI and data centers, it's no surprise that the mask industry has shown impressive strength—with a compound annual growth rate (CAGR) of 7.2% over the past seven years according to data available from SEMI.

JAN WILLIS

As we look ahead to 2025 and beyond, the future looks bright for the mask industry. According to experts who participated in the annual eBeam Initiative Luminaries survey, the results of which were released this past October, more than 90% anticipated increased purchases of multi-beam mask writers over the next three years, while more than 80% predicted increased purchases of mask inspection equipment over the same period. This optimism reflects the role of multi-beam mask writers in enabling the production of both EUV and curvilinear masks, and the role of mask inspection in maintaining the reliability of advanced photomasks. A large number of survey participants also predicted increased purchases of laser mask writers, which typically write the majority of photomasks each year, and are going through a replacement and expansion cycle.

Industry experts at an eBeam Initiative panel held in October underscored the significant role of multi-beam writers in writing EUV masks, with increasing demand tied to the global installation of EUV lithography systems. With multi-beam mask writers now widely deployed, there is an opportunity to take advantage of their ability to print any mask shape within the same write time and target more pervasive curvilinear mask shapes. Curvilinear inverse lithography technology (ILT) used to generate the target mask shapes is gaining traction, with over 70% of survey respondents acknowledging its potential utility for 193i nodes in addition to EUV. Curvilinear mask features have been shown not only to print more accurately, but also to print more reliably, which is good for both mask and wafer quality.

Increasing investments in critical photomask infrastructure yields benefits for the entire mask-to-wafer ecosystem. The future for the photomask industry is bright indeed, promising continued expansion and technological leadership in the years to come.

AI is the Driving Force

DALIA VERNIKOVSKY, CEO of ASNA

This year continues to anticipate the impact of AI as the driving force behind optimism in our industry. There is hardly a day that goes by without hearing about its ability to change our everyday lives and a pervasive presence in technological progression. This optimism has created the reason for the huge upward trend predicted in these coming years towards the one Trillion -dollar market most analysts are projecting. Yet making the chips that serve this technology must be dealt with at a practical and pragmatic level. We are excited to help participate in many of these manufacturing discussions – seeing both the use of newest platforms but also working on securing the supply chain resiliency as well as quality that must be respected throughout the process. In addition, the geo-political issues surrounding regulations, China being a prime example, can cripple forward progression. Without adequate resolution, there will be a continuance of doubt as to how well our upward trends will succeed in the short amount of time projected for success. Along with many challenges inclusive of PFAS restrictions and geo-political uncertainties, there are many obstacles that can slow this trend. Both the complexity of the manufacturing processes and without resilient supply chains (and a world that does not continue to place barriers to trade and huge taxation policies), some of the trend cycles will slow. There has already been a slow-down of fabrication sites to have been built and delays that will impact these opportunities . On the flip side, government recognition of the Semiconductor's importance will push us forward to building fabrication sites and bring back the idea of manufacturing in both the US as well as Europe versus moving everything to Asia in past trends

DALIA VERNIKOVSKY

As we watch the many developments, and also understand the importance of chips that serve our present, not only the future, ASNA will continue to educate and lead in the supply chain resilience

and quality required to meet the demands of global manufacturing and the huge challenges it faces.

New Packaging Approaches Drive Cost & Efficiency in 2025

JIM STRAUS, Vice President of Sales, ACM Research

The rapid demand for artificial intelligence (AI) and high-bandwidth memory (HBM) devices that can handle massive data processing and are large in size (~800 mm^2) is driving the industry transition to chiplets. While chiplets have been in use for decades, they've been employed sparingly and for very specific purposes. Now, they're at the cutting edge of technology for desktop PCs, workstations, and servers. Chiplets are segmented processors with specific sections manufactured as separate chips. These individual chips are then mounted together into a single package using a complex connection system.

JIM STRAUS

The fast adoption of chiplets will continue to drive wafer-level packaging (WLP) growth in 2025, as semiconductor companies continue to invest in various types of packages for diverse applications, including automotive, CMOS sensors, MEMS, RF filters, and more. These high-demand WLPs include die-to-die, die-to-wafer, wafer-to-wafer, and fan-out wafer-level packaging. However, the industry is experiencing capacity constraints due to the large size of these packages.

Panel-level packaging (PLP) has many advantages over WLP. PLP enables the industry to significantly increase the substrate area for building chiplets, improving yield and reducing packaging costs. The larger area allows more chips to be assembled at the same time, increasing capacity and reducing supply constraints. Fan-out panel-level packaging (FOPLP) allows for simplified integration of various die technologies (logic, memory, and RF) into a single package that is smaller and thinner.

PLP reduces compute times and power usage, supporting a more complex system for AI and high-performance computing (HPC) applications. As a result, we expect to see growing adoption of PLP in 2025. ACM Research is supporting the transition to PLP with new substrate handling systems and improved panel cleaning and deposition technologies. ACM Research is developing a panel cleaning tool that can remove flux and contamination from the center of the panel to eliminate void formation, as well as an electroplating tool that can provide uniform deposition across a 600mm square panel.

Addressing these technical challenges will be a major hurdle in 2025, helping to ease the transition to PLP, improve capacity, and support the chip demand for the AI and HPC applications of the future.

Opportunities Abound for Semiconductor Equipment in 2025

DR. ISMAIL KASHKOUSH, chief technology officer at JST Manufacturing

As we look ahead to 2025, we're seeing three major trends: a growing compound semiconductor market, the resurgence of wet bench technology and growing workforce development needs.

First, there is an increasing need for SiC and GaN equipment and process development to support the fast-growing AI, IOT, automotive, and aerospace markets – industries that are poised for growth. Process requirements for compound semi manufacturing are relatively less stringent than for a typical IC fab, which gives tool makers a golden opportunity to be strategic and develop tools specifically for this market. It also means equipment suppliers need to get creative by finding ways to reduce the cost of ownership while also making tools and processes more sustainable.

Second, while single wafer tools in state of-the-art 300 mm IC fabs are established in many process steps, there are still applications being performed in batches such as photoresist stripping, nitride etch, and wafer reclaim. Wet benches aren't going away for one simple reason: cost of ownership. Process flows in 150 and 200 mm CMOS fabs are still using batch processing to meet high throughput requirements (>250 wph). Many of these fabs are still using old tools quickly becoming obsolete, making parts and support hard to find, if the original tool makers still exist. This means these tools must be replaced. Again, tool makers must be innovative and develop new systems that use less water, require less exhaust, have smaller footprints, consume less energy and have a lower carbon footprint to meet increasing sustainability demands.

Third, talent acquisition is a prominent issue for the industry, especially in the U.S. and Europe markets, where product demand is high. Many new fabs are starting to ramp and in need of engineers, scientists, and technicians. With talent coming from a wide range of backgrounds, companies need to beef up their efforts to fill open positions and accelerate training programs so new hires are workforce ready. At JST Manufacturing, we're forging partnerships with technical colleges and universities as part of our recruitment solution with a focus on internships. This approach lays the foundation for students to meet their future employers and become familiar with the job quickly, and at a reasonable cost to us.

For us, we see these challenges as opportunities. Working with our customers will ensure we can support the growing needs for compound semiconductor manufacturing tools and new and improved wet bench and single wafer technologies, while working with our communities will help us fill the talent gap. With our lineup of single wafer and batch tools, we're excited to see where 2025 takes us.